We claim:

1. A method, comprising:

providing a first address containing a first number of bits and having an upper portion and a lower portion;

comparing the upper portion with a plurality of first entries in a first table;

if the upper portion matches a particular one of the plurality of first entries:

selecting a second entry in the first table associated with the particular one of the plurality of first entries;

combining the second entry with the lower portion to form a first translated address; and

transmitting the first translated address.

2. The method of claim 1, further comprising:

if the upper portion does not match any of the plurality of first entries in the first table:

accessing a second table having a plurality of third entries;

indexing the second table with the upper portion to identify a particular one of the plurality of third entries;

combining the particular one of the plurality of third entries with the lower portion to form a second translated address; and

transmitting the second translated address.

3. The method of claim 2, wherein the first table is contained in an input-output controller and the second table is contained in main memory.

4. The method of claim 2, wherein transmitting the first and second translated addresses includes transmitting to a memory controller.

5. The method of claim 1, wherein the first table is a translation lookaside buffer.

6. The method of claim 1, wherein providing a first address includes providing a first address from a bus controller.

7. The method of claim 6, wherein the first table is also used to translate addresses from a graphics controller.

8. A method, comprising:

using a conversion table to translate a first address from a graphics controller to a memory; and

using the conversion table to translate a second address from a bus controller to the memory.

9. The method of claim 8, wherein using the conversion table includes using a translation lookaside buffer.

10. The method of claim 8, wherein translating the second address includes translating the second address to a third address having a different number of bits than the second address.

11. The method of claim 10, wherein translating the first address includes translating the first address to a fourth address having a same number of bits as the first address.

12. The method of claim 8, wherein using the conversion table to translate the second address includes:

comparing a first portion of the second address with entries in a first table;

if the first portion matches a particular one of the entries in the first table,

combining a value associated with the particular one with a second portion of the second address to form a translated address.

13. The method of claim 12, further comprising:

if the first portion does not match any of the entries in the first table,

referring to a second table to translate the second address.

14. The method of claim 13, wherein:

comparing includes comparing the first portion of the second address with entries in a first table in an input-output controller; and

referring to the second table includes referring to the second table in main memory.

15. An apparatus, comprising:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of an initial address in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first translated address and hold the first translated address in the output register.

16. The apparatus of claim 15, wherein the control logic is further to:

access a table in memory if the matching entry is not found;

find a second value in the table associated with the first portion;

combine the second value with the second portion to form a second translated address: and

hold the second translated address in the output register.

17. The apparatus of claim 16, wherein:

the control logic includes logic for first and second control flows;

the first control flow is to translate an initial graphics controller address and does not access the second table; and

the second control flow is to translate an initial bus controller address and can access the second table.

18. The apparatus of claim 16, wherein the first and second translated addresses each have more bits than the initial address.

19. A system, including:

a processor;

a memory;

a graphics controller;

a bus controller;

an input-output controller coupled to the processor, memory, graphics controller and bus controller, the input-output controller including:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of an initial address in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first translated address and hold the first translated address in the output register.

20. The system of claim 19, wherein the control logic is further to:

access a table in memory if the matching entry is not found;

find a second value in the table associated with the first portion;

combine the second value with the second portion to form a second translated address; and

hold the second translated address in the output register.

21. The system of claim 20, wherein:

the control logic includes logic for first and second control flows;

the first control flow is to translate an initial graphics controller address and does not access the second table; and

the second control flow is to translate an initial bus controller address and can access the second table.

22. The system of claim 20, wherein the first and second translated addresses each have more bits than the initial address.

23. A machine-readable medium having stored thereon instructions, which when executed by a machine cause said processor to perform:

reading a first address containing a first number of bits and having an upper portion and a lower portion;

comparing the upper portion with a plurality of first entries in a first table;

if the upper portion matches a particular one of the plurality of first entries:

selecting a second entry in the first table associated with the particular one of the plurality of first entries;

combining the second entry with the lower portion to form a first translated address; and

transmitting the first translated address.

24. The medium of claim 23, further comprising:

if the upper portion does not match any of the plurality of first entries in the first table:

accessing a second table having a plurality of third entries;

indexing the second table with the upper portion to identify a particular one of the plurality of third entries;

combining the particular one of the plurality of third entries with the lower portion to form a second translated address; and

transmitting the second translated address.

25. The medium of claim 24, wherein the first table is contained in an input-output controller and the second table is contained in main memory.

26. The medium of claim 24, wherein transmitting the first and second translated addresses includes transmitting to a memory controller.

27. The medium of claim 23, wherein the first table is a translation lookaside buffer.

28. The medium of claim 23, wherein providing a first address includes providing a first address from a bus controller.

29. The medium of claim 28, wherein the first table is also used to translate addresses from a graphics controller.

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